NANO LETTERS
Letter
pubs.acs.org/NanoLett

Sub-10 nm Nanopattern Architecture for 2D Material Field-Effect Transistors

Kai Xu,[†,∥] Dongxue Chen,[†,⊥,#] Fengyou Yang,[†,∥] Zhenxing Wang,[†] Lei Yin,[†,∥] Feng Wang,[†,∥] Ruiqing Cheng,[†,∥] Kaihui Liu,[⊥] Jie Xiong,[*,§] Qian Liu,[*,†,‡] and Jun He[*,†]

[†]Chinese Academy of Sciences (CAS) Key Laboratory of Nanosystem and Hierarchy Fabrication, CAS Center for Excellence in Nanoscience, National Center for Nanoscience and Technology, Beijing 100190, China

[‡]The MOE Key Laboratory of Weak-Light Nonlinear Photonics, and TEDA Applied Physics Institute and School of Physics, Nankai University, Tianjin 300457, China

[§]State Key Laboratory of Electronic Thin Film and Integrated Devices, University of Electronic Science and Technology of China, Chengdu 610054, China

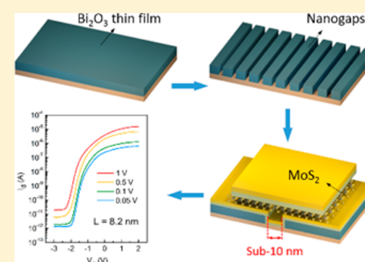
[∥]University of Chinese Academy of Sciences, Beijing 100080, China

[⊥]State Key Laboratory for Mesoscopic Physics, School of Physics, Peking University, Beijing 100871, China

[#]Department of Physics, South University of Science and Technology of China, Shenzhen 518005, China

Supporting Information

ABSTRACT: Two-dimensional materials (2DMs) are competitive candidates in replacing or supplementing conventional semiconductors owing to their atomically uniform thickness. However, current conventional micro/nanofabrication technologies realize hardly ultrashort channel and integration, especially for sub-10 nm. Meanwhile, experimental device performance associated with the scaling of dimension needs to be investigated, due to the short channel effects. Here, we show a novel and universal technological method to fabricate sub-10 nm gaps with sharp edges and steep sidewalls. The realization of sub-10 nm gaps derives from a corrosion crack along the cleavage plane of Bi_2O_3. By this method, ultrathin body field-effect transistors (FETs), consisting of 8.2 nm channel length, 6 nm high-k dielectric, and 0.7 nm monolayer MoS_2, exhibit no obvious short channel effects. The corresponding current on/off ratio and subthreshold swing reaches to 10^6 and 140 mV/dec, respectively. Moreover, integrated circuits with sub-10 nm channel are capable of operating as digital inverters with high voltage gain. The results suggest our technological method can be used to fabricate the ultrashort channel nanopatterns, build the experimental groundwork for 2DMs FETs with sub-10 nm channel length and 2DMs integrated circuits, and offer new potential opportunities for large-scale device constructions and applications.



KEYWORDS: *Sub-10 nm, nanopatterns, 2D materials, field-effect transistors, very-large-scale integration*

As the scaling of complementary metal-oxide-semiconductor (CMOS) silicon-based devices reaches its physical limits, many alternative channel materials and new technological approaches have been developed to decrease the transistors in size.[1−3] The current International Technology Roadmap for Semiconductors (ITRS) has predicted new materials and geometries are needed so as to solve the problems of transistor scaling during the next 10 years.[4] Especially, the channel length of 9.7 nm for high-performance technologies is proposed by ITRS 2012 for midterm (2021) nodes.[4]

Two-dimensional materials (2DMs), as one class of promising alternative channel materials,[5−7] own extra advantages such as atomic smoothness, uniform thickness and dangling bond-free surface, intrinsically suppressing trap generation, and surface scattering.[8] The most remarkable merit of 2DMs is their atomic thickness, which is immune to short channel effects (SCEs),[9] especially suitable for sub-10 nm channel length devices. In general, the channel thickness should be roughly less than one-third of the gate length to maintain effective gate electrostatics in field effect transistors (FETs).[10] Thus, the ultrashort gate length generated by the atomic thickness in 2DMs FETs ensures that the 2DMs FETs are excellent candidates in replacing and supplementing silicon-based CMOS.[11]

Currently, most 2DMs FETs are fabricated by electron beam lithography (EBL).[12] So far, multilayer MoS_2 FETs with 50 nm channel length have been demonstrated on 300 nm SiO_2 by using EBL.[13] However, fabrication of smaller channel length especially sub-10 nm has always kept a significant challenge because of some restrictions coming from e-beam resist, EBL process, and lift-off process.[14,15] New technological routes for transistors scaling are desired due to shortage of the

Received: November 2, 2016
Revised: December 20, 2016
Published: January 16, 2017

ACS Publications © 2017 American Chemical Society

DOI: 10.1021/acs.nanolett.6b04576
Nano Lett. 2017, 17, 1065−1070

conventional micro/nanofabrication. Recently, MoS_2 FETs adopted a carbon nanotube of 1 nm diameter as gate electrode show good switching characteristics,[5] but the distance between source and drain is still several hundred nanometers, and this smart method is not actually appropriate for integration of devices for very-large-scale integration (VLSI). Actually, 2DMs devices still have many obstacles in order to reach goal in ITRS, such as fabrication method of sub-10 nm channel length for decreasing the transistors in size, sub-10 nm gap with sharp edges and steep sidewalls for high-performance FETs, being capable of naturally compatible with planar technologies for VLSI, using high-*k* dielectric as gate dielectric layer for smaller 2DMs device, and so forth. This means that it is impossible by conventional micro/nanofabrication technologies to realize ultrashort channel and integration therein at the same time.

Taking MoS_2 as an example, here we demonstrate a novel and universal technological method, which can fabricate 2DMs FETs with sub-10 nm channel with sharp edges and steep sidewalls and realize the integrated circuits based on 2DMs. The electrical transport investigation of ultrathin body MoS_2 FETs (8.2 nm channel length, 6 nm high-*k* dielectric, and 0.7 nm monolayer MoS_2 thickness) shows a current on/off ratio up to 10^6 and a subthreshold swing of 140 mV/dec. Moreover, the monolayer MoS_2 FETs do not exhibit obvious short channel effects. More importantly, corresponding integrated circuits based on the sub-10 nm channel are demonstrated by means of a digital inverters with high gain. Our results suggest that the fabrication method can be used as an alternative approach for 2DMs integrated circuits and has great potential for surpassing the performance of established technologies, and this will open many opportunities for new devices and applications.

The sub-10 nm gap with high aspect ratios is a great challenge in fabrication. For the current conventional nanofabrication techniques, achieving so thin nanogap with sharp edges and steep sidewalls is almost impossible.[16] Here we present a simple realizing method based on a corrosion cracking along with the cleavage plane of the bismuth trioxide (β-Bi_2O_3). As shown in Figure 1 and Supplementary Figure S1, β-Bi_2O_3 film is first deposited on silicon wafer by magnetron sputtering. Subsequently, the β-Bi_2O_3 film is annealed at 350 °C in ambient, and the crystalline domains of the β-Bi_2O_3 film in a range of tens to hundreds micrometers are obtained. Due to the difference of expansion coefficient between the silicon and the β-Bi_2O_3, stress exists between substrate and crystallographic films during annealed process, and then the annealed β-Bi_2O_3 film is immersed into dilute nitric acid (HNO_3). Synergistic effect of stress and corrosion results in parallel gaps along with the cleavage plane of every crystal domain (Figure 1a). Scanning electron microscope (SEM) image of the parallel and quasi-periodic nanogaps is shown in Figure 1b. The corresponding standard deviation from a quasi-periodic array of nanogaps is estimated to be 140 nm. High-resolution transmission electron microscope (TEM) image (Figure 1c) and selected area electron diffraction pattern of the area with dotted box in Figure 1c indicate that the milled face is plane {001} and the cracking plane of β-Bi_2O_3 is plane {110}.

In addition, the thickness of the β-Bi_2O_3 film can be well controlled by magnetron sputtering time, and the width of the nanogaps can be regulated by etching time in HNO_3 solution (Figure 1e). The study for dependence of width on etching time is further carried out, as shown in Figure S2. The widths of nine gaps in the same crystalline domain are examined with etching times ranging from 10 to 130 s (Figure S2d). The width

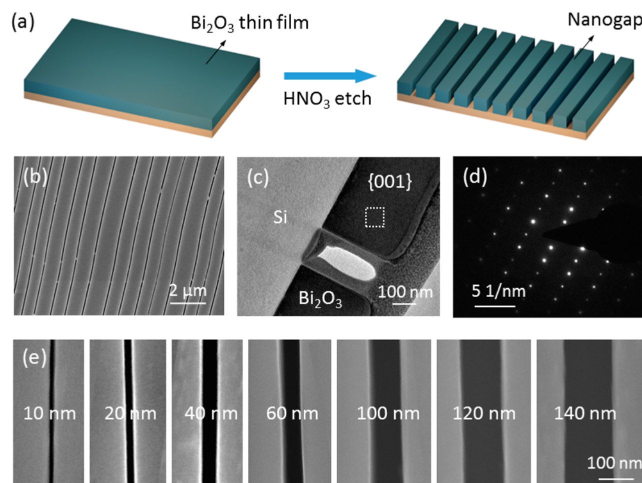


Figure 1. Novel method to fabricate parallel and quasi-periodic nanogaps. (a) Schematic diagram of nanogaps fabrication process. (b) SEM image of parallel and quasi-periodic nanogaps. (c) Cross-section TEM of nanogaps with straight and steep sidewalls, resulting from synergistic effect of stress and corrosion. (d) SAED pattern indicates milled face is plane {001}, and cracking plane of β-Bi_2O_3 is plane {110}. (e) The width of nanogaps can be tunable in the range of several to hundred nanometers. The nanogaps pattern fabricated by the novel method is large-scale, parallel, quasi-periodic, and straight, providing new opportunities for large-scale device constructions and applications.

of gaps can be modulated by varying etching time, and the average etching speed is extracted to be 1.9 nm/s. The width of nanogaps is in the range of several to hundred nanometers, and the minimum width can be achieved about 5 nm (Figure S1c). Sub-10 nm gaps spacing are also measured by the high-resolution AFM, as shown in Figure S3. It clearly demonstrates that the width of gap is 7 nm (Figure S3f). More importantly, compared with high-resolution AFM, SEM image for the same gap also shows about 7 nm spacing, indicating reliability of our SEM measurement. In our experiments, 300 nm Bi_2O_3 film is used to fabricate sub-10 nm nanogaps. The formation mechanism of nanogaps is probably divided into two stages. At the beginning of the formation of nanogaps, stress dominates the cracking process. Actually, the nanogaps with few nanometers width will develop spontaneously if the Bi_2O_3 film is placed in ambient for a long time. With HNO_3 accelerating stress release, nanogaps will develop rapidly. After the stress is released, HNO_3 corrosion is the prominent effect to broaden the nanogaps. It should be noted that the parallel, quasi-periodic and straight nanogaps pattern is capable of large-scale fabrication, providing us more opportunities for large-scale devices and applications.

The ultrashort channel devices are fabricated on the β-Bi_2O_3 sub-10 nm gaps (Figure 2a). To avoid the influence of the β-Bi_2O_3 on electrical properties of device, high-*k* dielectric HfO_2 thin film is deposited on β-Bi_2O_3 film by atomic layer deposition (ALD) (Figure 2b). It is noted that HfO_2 can not only guarantee robust device performance but also regulate the width of nanogaps so as to further narrow channel. The electrical contact patterns are defined by electron beam lithography (EBL), and 5 nm Au is deposited using magnetron sputtering (Figure 2c). Then, as-grown monolayer MoS_2 on SiO_2 is covered with poly(methyl methacrylate) (PMMA) as supporting layer by spin-coating method and soaked in potassium hydroxide (KOH) solution. The SiO_2 layer is etched

DOI: 10.1021/acs.nanolett.6b04576
Nano Lett. 2017, 17, 1065−1070

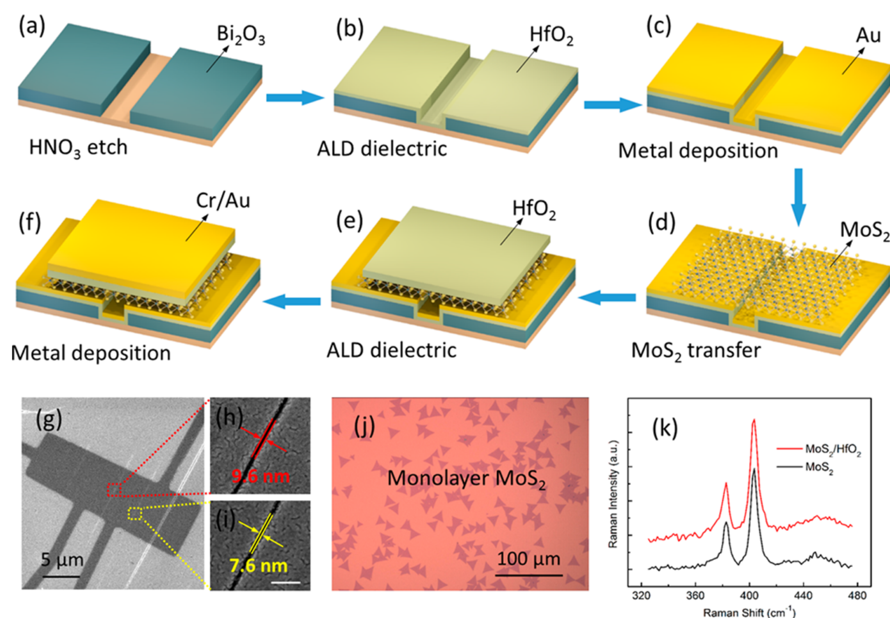


Figure 2. Fabrication process and characteristics of ultrashort channel devices. (a–f) Schematic diagrams of fabrication process of sub-10 nm channel length devices. (g–i) SEM images of device with 9.6 and 7.6 nm channel length. The magnetron sputtering plays a nonnegligible function during fabrication of the sub-10 channel length in our experiments. The scale bar is 10 nm. (j) Monolayer MoS_2 was synthesized by a typical chemical vapor deposition (CVD) method using MoO_3 and sulfur powder as precursors. The size of grown MoS_2 nanosheet is about 20 μm. (k) Raman spectra of pure MoS_2 and MoS_2 with Al and HfO_2 are obtained using 532 nm laser, exhibiting no shift among all samples and implying this method does not result in obvious damage or bond-disorder into MoS_2.

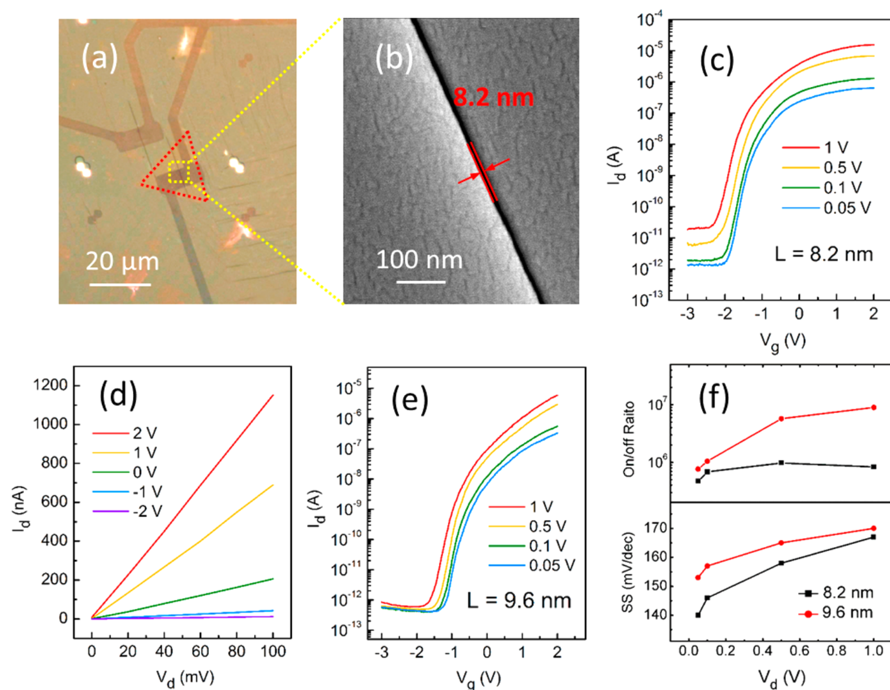


Figure 3. MoS_2 FETs with sub-10 nm channel length. (a) SEM and (b) optical image of monolayer MoS_2 FETs before fabrication of top-gate electrode, which indicates the channel length is about 8.2 nm. (c) Transfer and (d) output characteristics of monolayer MoS_2 FETs. The device exhibits no obvious short channel effect. (e) Transfer characteristics of multilayer MoS_2 FETs with 9.6 nm channel length. (f) Comparison of SS and current on/off ratio between monolayer and multilayer MoS_2 FETs.

away and the PMMA with MoS_2 is released and transferred to the target substrate (Figure 2d). After the transfer process, the devices are annealed at 180 °C for 3 h in argon atmosphere. Six nanometer-thick HfO_2 layer deposited by ALD is used as gate dielectric (Figure 2e), and the top gate electrode is then formed using a stack of 8 nm Cr and 40 nm Au after the gate pattern is conducted by EBL (Figure 2f).

Figure 2g shows the SEM image of a sample with two sub-10 nm channel length. The widths of two nanogaps are 9.6 and 7.6 nm, respectively, which is evident by gap details in the magnifying SEM image in Figure 2h,i. Actually, the magnetron

DOI: 10.1021/acs.nanolett.6b04576
Nano Lett. 2017, 17, 1065–1070

sputtering plays a critical function during fabrication of the sub-10 channel length in our experiments. The magnetron sputtering can usually form smaller Au particles than thermal evaporation, ensuring two contacts would not connect together in our geometry. The dependence of conductivity of Au film on magnetron sputtering time are displayed in Figure S4. The contacts were first deposited by thermal evaporation. However, due to the relatively larger Au particles in thermal evaporation, two electrodes are easy to connect together. Further, the sub-10 nm nanogaps fabricated by our method exhibit excellent uniformity along the micrometer-long nanogaps, as shown in Figure S5. Monolayer MoS_2 in our experiment was synthesized by a typical chemical vapor deposition (CVD) method using MoO_3 and sulfur powder as precursors.[17] The size of grown MoS_2 nanosheet is about 20 μm. However, to maintain effective gate electrostatics in ultrashort channel top-gate FETs, ultrathin 6 nm high-*k* HfO_2 is chosen as gate dielectric with equivalent oxide thickness (EOT) of 2 nm in our experiment. However, owing to the absence of dangling bonds of MoS_2, there are many challenges in the deposition of HfO_2 dielectric directly on MoS_2 surface. Previous works on top-gate high-*k* dielectric MoS_2 FETs focus on relatively thick dielectric such as 50 nm Al_2O_3 and 30 nm HfO_2,[12,18] and sub-10 nm thickness dielectrics in MoS_2 FETs are rarely covered. Actually, without any modification on MoS_2 surface, ultrathin HfO_2 dielectric film forms discontinuous layers with pinhole defects, especially for sub-10 nm atomic layer deposited by ALD.[19] To ensure the growth of high-quality HfO_2, 1.5 nm aluminum (Al) as a buffer layer is deposited on the MoS_2 surface by thermal evaporation. As displayed in Figure 2k, Raman spectra of pure MoS_2 and MoS_2 with Al and HfO_2 are obtained using 532 nm laser. Two prominent peaks of MoS_2, 383 and 403 cm^{-1}, exhibit no shift among all samples, implying this method does not result in obvious damage or bond-disorder into MoS_2.

Figure 3a,b displays the optical image and SEM image of monolayer MoS_2 devices before fabrication of top-gate electrode, which indicates the channel length is about 8.2 nm. The corresponding transfer and output curves are presented in Figure 3c,d. For this device, the current on/off ratio is approximately 10^6 for drain voltage (V_d) = 0.5 V and is able to maintain 8×10^5 for V_d = 1 V. Benefiting from its ultrathin body structure (monolayer MoS_2, 6 nm HfO_2), the current on/off ratio dose not degenerate much, indicating a good immunity to SCEs. The channel length of 9.7 nm for high-performance technologies is proposed by ITRS 2012 for midterm (2021) nodes.[4] Sub-10 nm channel length of our MoS_2 FETs is beyond the range of conventional MOSFETs. To estimate the occurrence of SCEs in our devices, channel length L and characteristic length λ need to be compared.[3] The characteristic length of MOSFETs with planar structure is given by $\lambda = (\varepsilon_s/\varepsilon_{ox}t_st_{ox})^{1/2}$, where ε_s and ε_{ox} are the dielectric constant of semiconductor and gate oxide, and t_s and t_{ox} are the thickness of semiconductor and gate oxide, respectively. Generally, in order to maintain effective gate electrostatics, channel length L should be >2.5 times larger than characteristic length λ. Actually, the superior immunity to SCEs derives from not only its ultrathin body feature but also its relatively low dielectric of MoS_2. According to previous reports, the dielectric constant of MoS_2 is about 3.3.[20] The characteristic length for monolayer MoS_2 FETs with 6 nm HfO_2 as dielectric is 1.2 nm, which is far below 10 nm node for alternative channel materials for logic applications. Thus, the sub-10 nm MoS_2 FETs in our experiment do not exhibit obvious SCEs. The on-state current is over 2.5 μA/μm at V_d = 1 V, and the off-state current is 3 pA/μm. Although the on-state current is lower than what ITRS needs for high-performance (HP) technologies, the off-state current is desirable for low-power (LP) logic requirements (100 nA/μm). Besides, due to absence of dangling bonds on 2DMLs surface, it is difficult to directly integrate robust high-*k* HfO_2 dielectric on 2DMs, especially sub-10 nm thickness. By utilizing Al as a buffer layer, 6 nm thickness HfO_2 film is achieved on monolayer MoS_2 surface. The gate current of this ultrathin body device is in the range of pA, as shown in Figure S6.

Considering monolayer MoS_2 owns a larger bandgap,[21] thus, a lower mobility and larger contact resistance than multilayer MoS_2,[22] a multilayer MoS_2 (4 nm) FETs with 9.6 nm channel length was fabricated for a better device performance (Figure S7). Figure 3e displays the transfer characteristic of this transistor. The current on/off ratio is about 9×10^6 for V_d = 1 V, larger than that of monolayer MoS_2 FETs with 8.2 nm channel length, as shown in Figure 3f. For this device, the characteristic length is calculated to be 3.3 nm and the channel length is >2.5 times larger than this value. Thus, we also do not observe obvious SCEs in this multilayer MoS_2 FETs with sub-10 nm channel length. The on-state current (2.7 μA/μm) and off-state current (0.3 pA/μm) at V_{ds} = 1 V are also superior to the values of monolayer MoS_2 FETs. Further, the subthreshold swing (SS) is introduced to characterize the rate of increase of the drain current under the gate voltage and can be given by SS = $dV_g/d(l_g(I_d))$, where V_g is the gate voltage and I_d is the drain current. The SS of two ultrashort channel FETs are compared under different drain voltage, as plotted in Figure 3f. The SS of both devices vary in the range of 140−170 mV/dec, and the smallest SS of 140 mV/dec is achieved in monolayer MoS_2 FETs. The current on/off ratio of 10^6, SS of 140 mV/dec, and low off-state current of 3 pA/μm correspond to previous ultrashort channel MoS_2 devices.[23] The SS of the monolayer MoS_2 FETs are smaller than that of multilayer MoS_2 FETs due to better control of gate electrostatics in monolayer MoS_2 FETs.

As we know, in low electric field (low drain voltage), the velocity of carrier increases almost linearly with electric field increasing, leading to constant mobility. In very high electric field, the velocity would saturate, especially for ultrashort channel. Besides, for high on-state gate voltage, the contact resistance would reduce to minimum, compared with off-state gate voltage. Thus, in the case of low electric field and constant mobility, the mobility can be calculated in high gate voltage and low drain voltage to minimize the contact resistance (V_g = 2 V, V_d = 0.05 V). The mobility is estimated by the equation $\mu = L/(W(\varepsilon_o\varepsilon_r/d)V_d)(dI_d/dV_g)$. The value of mobility (V_g = 2 V, V_d = 0.05 V) in multilayer device is 1.1 $cm^2\ V^{-1}\ s^{-1}$. However, in the case of high electric field and velocity saturation, the saturation current can be estimated by the following equation: $I_{dsat} = WC_{ox}(V_g - V_t)\nu_{sat}$. The saturation velocity is calculated to be 1×10^5 cm/s, consistent with previous results.[7] Actually, the calculated mobility and saturation velocity should be underestimated. There are mainly several reasons for this relatively low mobility. (1) In the CVD process of monolayer MoS_2, defect states of monolayer MoS_2 itself are inevitable and have a great impact on the device performance, especially compared with multilayer MoS_2. (2) The deposition of 1.5 nm Al on the surface of MoS_2 leads to some Coulomb scattering and roughness scattering. However, without Al as buffer layer, the high-*k* dielectric deposited on MoS_2 surface develops discontinuous film, especially sub-10 nm thickness.

DOI: 10.1021/acs.nanolett.6b04576
Nano Lett. 2017, 17, 1065−1070

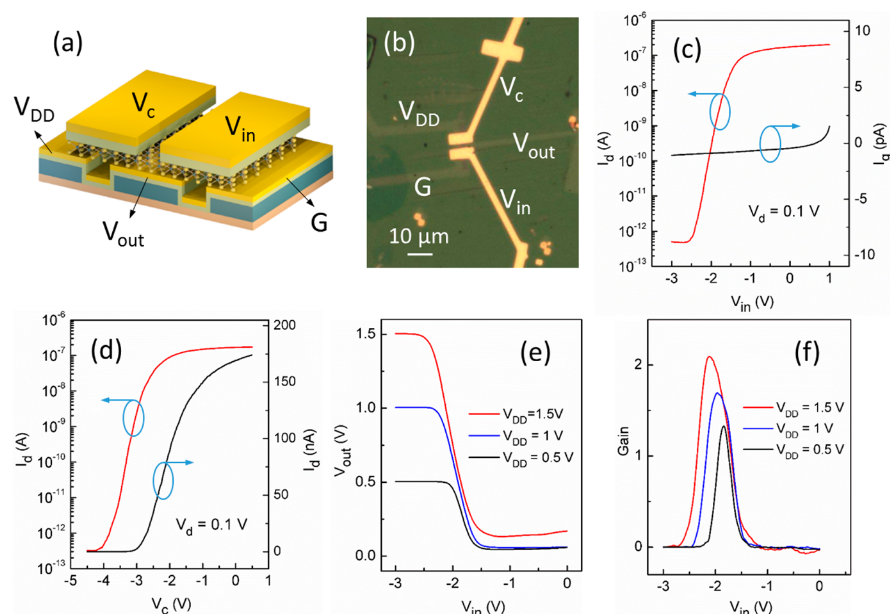


Figure 4. Integrated digital inverter. (a) Schematic diagram of an inverter structure consisting of two n-type MoS_2 with sub-10 nm channel. (b) Optical image of a typical inverter device. The "upper transistor" and "lower transistor" can be independently controlled by corresponding top-gate electrodes. (c) The transfer characteristic and gate current of "lower transistor". The gate current (I_g) is found to be less 2 pA, which attribute to the buffer layer between channel materials and HfO_2. (d) The transfer characteristic of "upper transistor". (e) Output voltage as a function of input voltage at different supply voltages. (f) Dependence of the inverter gain on the input voltage and supply voltage. The maximal voltage gain is above 2, indicating our inverter based on ultrashort channel FETs is suitable for integration in arrays of logic devices.

Logic circuits and amplification of electrical signals construct the cornerstone of modern electronics. We have demonstrated atomic layer MoS_2, a typical 2DM, offers a higher degree of electronic control than bulk materials and represents ultimate limit of miniaturization of electronic circuits. The tunable nanogaps pattern provides a new approach of integration of 2DMs for miniaturization. Our integrated circuit, a 2D digital inverter, consists of two sub-10 nm transistors realized on the same multilayer MoS_2, as schematically displayed in Figure 4a. These two transistors are connected in series, and meanwhile both of them can be independently controlled by corresponding top-gate electrodes. Actually, it is essential for constructing integrated circuits of multiple transistors on the same chip. Figure 4c,d presents the transfer characteristic of "lower transistor" and "upper transistor" and the drain current can be modified with on/off ratio of 10^6 by top-gate voltage at V_d = 0.1 V. This effective gate electrostatics control is imperative for realizing digital inverter with large voltage gain. Besides, as shown in Figure 4c, the gate current (I_g) is found to be less than 2 pA, which attributes to the buffer layer between channel materials and HfO_2.

We further demonstrated that our integrated circuit can operate as a logic inverter, the most basic logic component. In this configuration depicted in Figure 4b, the "lower transistor" operates as switch, and the "upper transistor" as effective load is applied by a constant voltage (V_c = −1 V). The supply voltage (V_{DD}) is applied to drain electrode. Input voltage (V_{in}) is applied to the top-gate electrode of "lower transistor" and output voltage (V_{out}) is the function of V_{in} and V_{DD}. For input voltage below −2.5 V, corresponding to logic 0, the "lower transistor" owns a higher resistance than "upper transistor", which results in the output voltage close to the supply voltage, donating logic 1. For input voltage above −1.5 V, corresponding to logic 1, the switch transistor is more conductive and the output voltage remains in the range of low voltage, as shown in Figure 4e. As the most important parameter, the gain of inverter is defined as $-dV_{out}/dV_{in}$. For the input voltage ranging from −2.5 V to −1.5 V, the output voltage changes faster than the input voltage, and the gain reaches 2.1 when V_{DD} = 1.5 V (Figure 4f). Actually, for successful realization of digital inverter based on new materials, the gain larger than the unity gain (gain = 1) is essential so that the output voltage can drive the next inverter in the cascade.[24]

The realization of sub-10 nm channel devices derives from our nanogaps with sharp edges and steep sidewalls, which have an atomic smooth level theoretically due to gaps along the cleavage plane of the β-Bi_2O_3 crystal. Whereas it almost impossible at such scale for current conventional micro/nanofabrication technologies. This simple fabrication method of the nanogaps is capable of naturally compatible with planar technologies for VLSI. Moreover, the ultrathin body MoS_2 FETs as a reference sample have been successfully built based on the sub-10 nm gaps. Such FETs consisting of 8.2 nm channel length and 6 nm-thick high-k dielectric can obviously satisfy size requirement of a channel length down to 10 nm in ITRS. The current on/off ratio of the FETs reaches to 10^6 larger than the requirement for practical application (10^4), indicating this device is practical for future device generations. We also demonstrated operable inverter integrated sub-10 nm devices into circuits, providing a road to solve long channel 2DMLs transistors that are unable to compete with the circuits based on silicon transistors.

Summarizing, we have designed a novel and universal method to fabricate ultrashort channel FETs and integrated circuits with sub-10 nm channel length. As a reference sample, monolayer MoS_2 FETs with 8.2 nm channel length and 6 nm high-k HfO_2 show no obvious short channel effect. The current on/off ratio of 10^6 and SS of 140 mV/dec are achieved successfully. Moreover, multilayer MoS_2 (4 nm) FETs with 9.6 nm channel length exhibit better performance than monolayer

DOI: 10.1021/acs.nanolett.6b04576
Nano Lett. 2017, 17, 1065−1070

MoS_2 FETs. Finally, we successfully constructed and demonstrated a digital inverter device composed of ultrashort channel MoS_2 FETs with high gain of 2.1 at supply voltage of 1.5 V. Our finds supply experimental guidelines for 2DM FETs with sub-10 nm channel length offer an exciting route for designing novel devices and applications and open up many opportunities for VLSI in the future.

Methods. A β-Bi_2O_3 film is deposited by magnetron sputtering (Kurt J. Lesker, PVD75, Ar 20 sccm, O_2 5 sccm, 10^{-8} Torr base pressure, 50 W, 232 V) with a β-Bi_2O_3 target. The typical thickness of β-Bi_2O_3 film is 300 nm. The β-Bi_2O_3 film is annealed at 350 °C for 180 min in ambient and immersed in HNO_3 solution several seconds. The nanogaps are further characterized by SEM (Hitachi-4800) and TEM (FEI, F20). Monolayer MoS_2 nanosheets are synthesized by CVD method and transferred to the β-Bi_2O_3 film. Multilayer MoS_2 nanosheets (2D materials) are mechanically exfoliated from bulk MoS_2 and transferred to the β-Bi_2O_3 film using a previous reported transfer method.[25] HfO_2 thin film is deposited by ALD using KE-MICRO TALD-100A system. The electrical contacts are defined by standard EBL, and Au (5 nm) electrodes are deposited by magnetron sputtering. The Al nanoparticles are deposited using a thermal evaporation machine. The electrical measurements are performed on a probe station (Lakeshore TTP4) equipped with a vacuum pump and a semiconductor characterization system (Keithley 4200).

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.6b04576.

Nanogaps of β-Bi_2O_3 film. Dependence of conductivity of Au film on magnetron sputtering time. Excellent uniformity of the sub-10 nm nanogaps. The gate current curves of MoS_2. Characterization of multilayer MoS2 FETs (PDF)

■ AUTHOR INFORMATION

Corresponding Authors

*E-mail: hej@nanoctr.cn.

*E-mail: liuq@nanoctr.cn.

*E-mail: jiexiong@uestc.edu.cn.

ORCID

Jun He: 0000-0002-2355-7579

Author Contributions

K. X., D. C. and F. Y. contributed equally. The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

This work was supported by Ministry of Science and Technology of China (Nos. 2016YFA0200700 and 2016YFA0200403), National Natural Science Foundation of China (Nos. 21373065, 61474033, 61574050, 11674072, and 10974037), and Strategic Priority Research Program of the Chinese Academy of Sciences (Nos. XDA 09040201 and XDA 09020300). The authors also gratefully acknowledge the support of Youth Innovation Promotion Association CAS.

■ REFERENCES

(1) Franklin, A. D. *Science* **2015**, *349*, 6249.

(2) Chau, R.; Doyle, B.; Datta, S.; Kavalieros, J.; Zhang, K. *Nat. Mater.* **2007**, *6*, 810−812.

(3) Cao, W.; Kang, J. H.; Sarkar, D.; Liu, W.; Banerjee, K. *IEEE Trans. Electron Devices* **2015**, *62*, 3459−3469.

(4) International Technology Roadmap for Semiconductors (ITRS, 2012). http://www.itrs.net/.

(5) Desai, S. B.; Madhvapathy, S. R.; Sachid, A. B.; Llinas, J. P.; Wang, Q.; Ahn, G. H.; Pitner, G.; Kim, M. J.; Boker, J.; Hu, C.; et al. *Science* **2016**, *354*, 99−102.

(6) Guerriero, E.; Polloni, L.; Bianchi, M.; Behnam, A.; Carrion, E.; Rizzi, L. G.; Pop, E.; Sordan, R. *ACS Nano* **2013**, *7*, 5588−5594.

(7) Zou, X. M.; Wang, J. L.; Chiu, C. H.; Wu, Y.; Xiao, X. H.; Jiang, C. Z.; Wu, W. W.; Mai, L. Q.; Chen, T. S.; Li, J. C.; et al. *Adv. Mater.* **2014**, *26*, 6255−6261.

(8) Radisavljevic, B.; Kis, A. *Nat. Mater.* **2013**, *12*, 815−820.

(9) Sarkar, D.; Xie, X. J.; Liu, W.; Cao, W.; Kang, J. H.; Gong, Y. J.; Kraemer, S.; Ajayan, P. M.; Banerjee, K. *Nature* **2015**, *526*, 91−95.

(10) Zhang, F.; Appenzeller, J. *Nano Lett.* **2015**, *15*, 301−306.

(11) Liu, L. T.; Lu, Y.; Guo, J. *IEEE Trans. Electron Devices* **2013**, *60*, 4133−4139.

(12) Radisavljevic, B.; Radenovic, A.; Brivio, J.; Giacometti, V.; Kis, A. *Nat. Nanotechnol.* **2011**, *6*, 147−150.

(13) Liu, H.; Neal, A. T.; Ye, P. D. *ACS Nano* **2012**, *6*, 8563−8569.

(14) Miao, J. S.; Zhang, S. M.; Cai, L.; Scherr, M.; Wang, C. *ACS Nano* **2015**, *9*, 9236−9243.

(15) Radisavljevic, B.; Whitwick, M. B.; Kis, A. *ACS Nano* **2011**, *5*, 9934−9938.

(16) Pons, A. J. *Nature* **2012**, *485*, 177−178.

(17) van der Zande, A. M.; et al. *Nat. Mater.* **2013**, *12*, 554−561.

(18) Pezeshki, A.; Shokouh, S. H. H.; Raza, S. R. A.; Kim, J. S.; Min, S. W.; Shackery, I.; Jun, S. C.; Im, S. *J. Mater. Chem. C* **2014**, *2*, 8023−8028.

(19) Yang, W.; Sun, Q. Q.; Geng, Y.; Chen, L.; Zhou, P.; Ding, S. J.; Zhang, D. W. *Sci. Rep.* **2015**, *5*, 11921.

(20) Yoon, Y.; Ganapathi, K.; Salahuddin, S. *Nano Lett.* **2011**, *11*, 3768−3773.

(21) Mak, K. F.; Lee, C.; Hone, J.; Shan, J.; Heinz, T. F. *Phys. Rev. Lett.* **2010**, *105*, 136805.

(22) Allain, A.; Kang, J. H.; Banerjee, K.; Kis, A. *Nat. Mater.* **2015**, *14*, 1195−1205.

(23) Nourbakhsh, A.; Zubair, A.; Sajjad, R. N.; Amir, T. K. G.; Chen, W.; Fang, S.; Ling, X.; Kong, J.; Dresselhaus, M. S.; Allain, A.; et al. *Nano Lett.* **2016**, *16*, 7798−7806.

(24) Liu, E. F.; Fu, Y. J.; Wang, Y. J.; Feng, Y. Q.; Liu, H. M.; Wan, X. G.; Zhou, W.; Wang, B. G.; Shao, L. B.; Ho, C. H.; et al. *Nat. Commun.* **2015**, *6*, 6991.

(25) Dean, C. R.; Young, A. F.; Meric, I.; Lee, C.; Wang, L.; Sorgenfrei, S.; Watanabe, K.; Taniguchi, T.; Kim, P.; Shepard, K. L.; Hone, J. *Nat. Nanotechnol.* **2010**, *5*, 722−726.

DOI: 10.1021/acs.nanolett.6b04576
Nano Lett. 2017, 17, 1065−1070